Electronics, Data Acquisition, and Instrument Control

Henrik von der Lippe

LBNL

January 2001

Overview

Readout electronics — development activity:
- **GigaCam – 150 CCDs with 4-corner readout - 600 channels.**
- **NIRcam – up to 4 HgCdTe devices with 4-corner readout - 16 channels**
- **Spectrographs – up to 4 devices, 2 CCDs and 2 HgCdTe .**
- **Low power and small space highly desirable in a satellite.**
- **Judicious use of ASICs where most benefit is derived.**
- **Build proof-of-principle system prototype.**

DAQ — study and tradeoff activities:
- **Compress, buffer and transmit all exposures.**
- **Look for existing solutions, but we do have unique issues.**
- **Preparation for informed conversations with our spacecraft team, consultants and vendors.**

Instrument Controls — study and tradeoff activities :
- **Device readouts have configuration parameters: modes, voltage levels, etc.**
- **Instruments have mechanisms that need to be cycled.**
- **Instruments may have internal monitoring information that needs to be collected.**

Science driven requirements

Sensor read noise limited – readout chain contribution must be small.

Readout rate compatible with 20 second readout time – implies approximately 100 kHz pixel rate.

Data buffer size and telemetry bandwidth must not impact the observation program.

Fine grain failure isolation at readout level and redundancy at the data collection level – insure operational lifetime.

R&D

Readout electronics

- Requirements development.
- Implementation concepts - common solutions
- Identify ASICs
- Two cycles of ASIC development
- Construct a prototype readout system.

On board data acquisition

- How to collect data streams on board.
- What to do with the collected data on board.

Instrument Controls

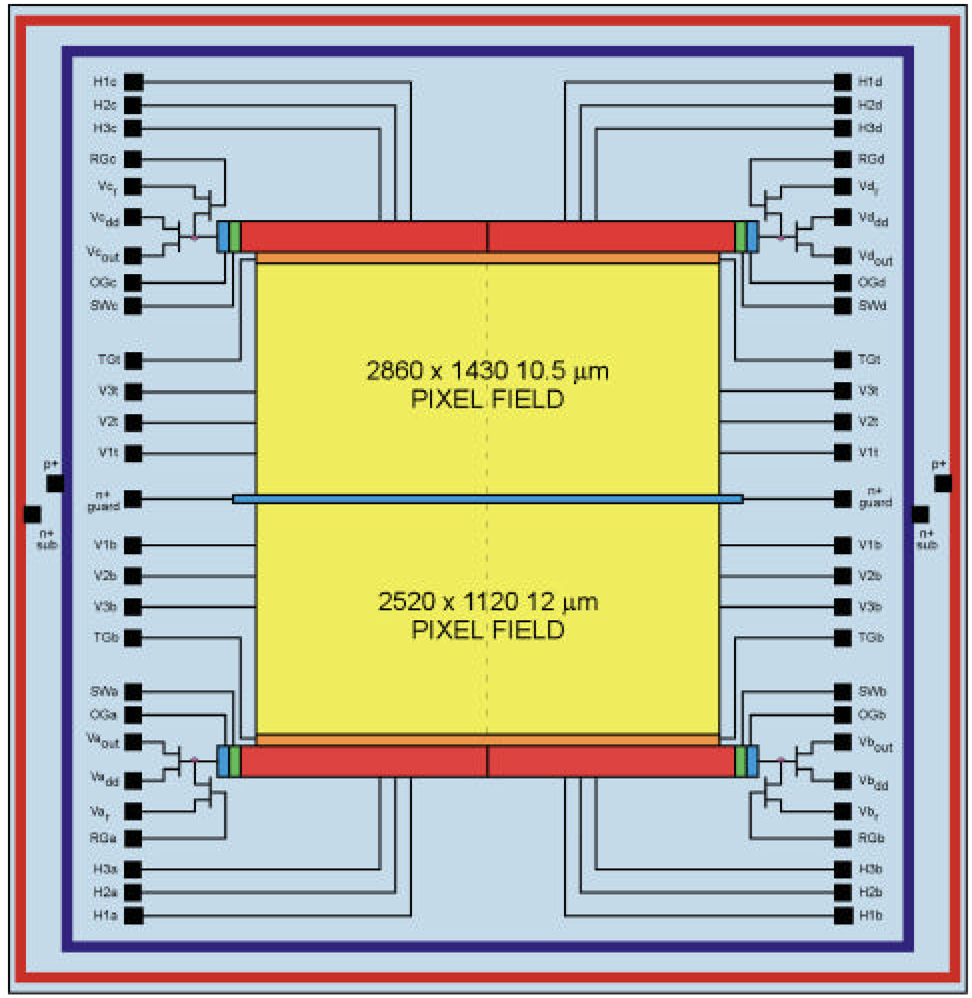
- What are instrument control needs.
- What instrument health monitoring is needed.
- How is the observation program directed from ground.

SNAP CCD Concept

2 x 2860 x 1430 10.5 mm
or
2 x 2520 x 1120 12.0 mm

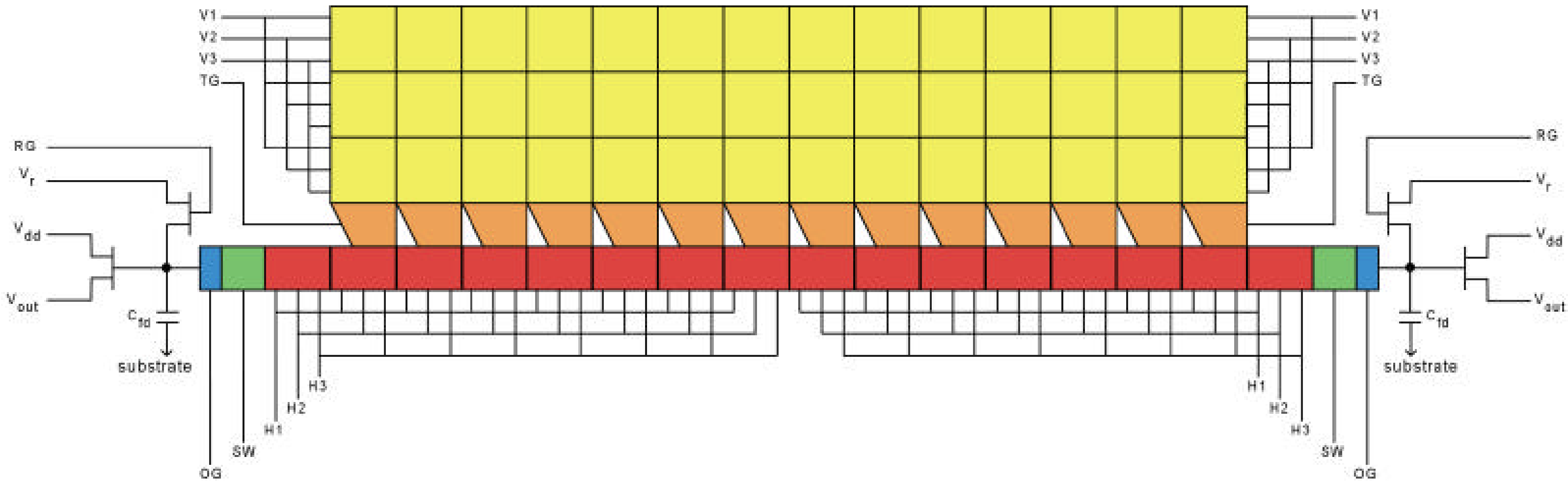
4-corner and 2-corner readout.

Read noise as low as 2 e.
Sensitivity as high as 6 mV/e.



CCD Control Signals

The figure is an abstraction of the serial register neighborhood.

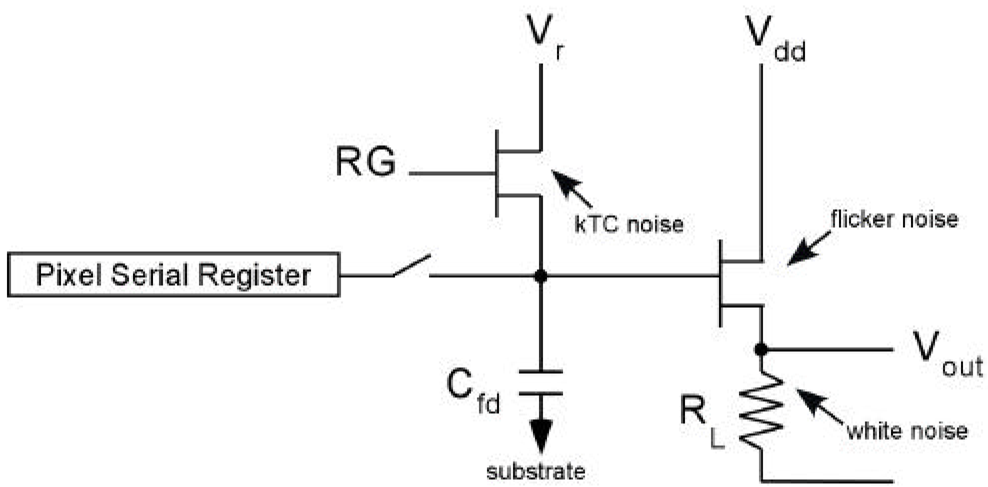


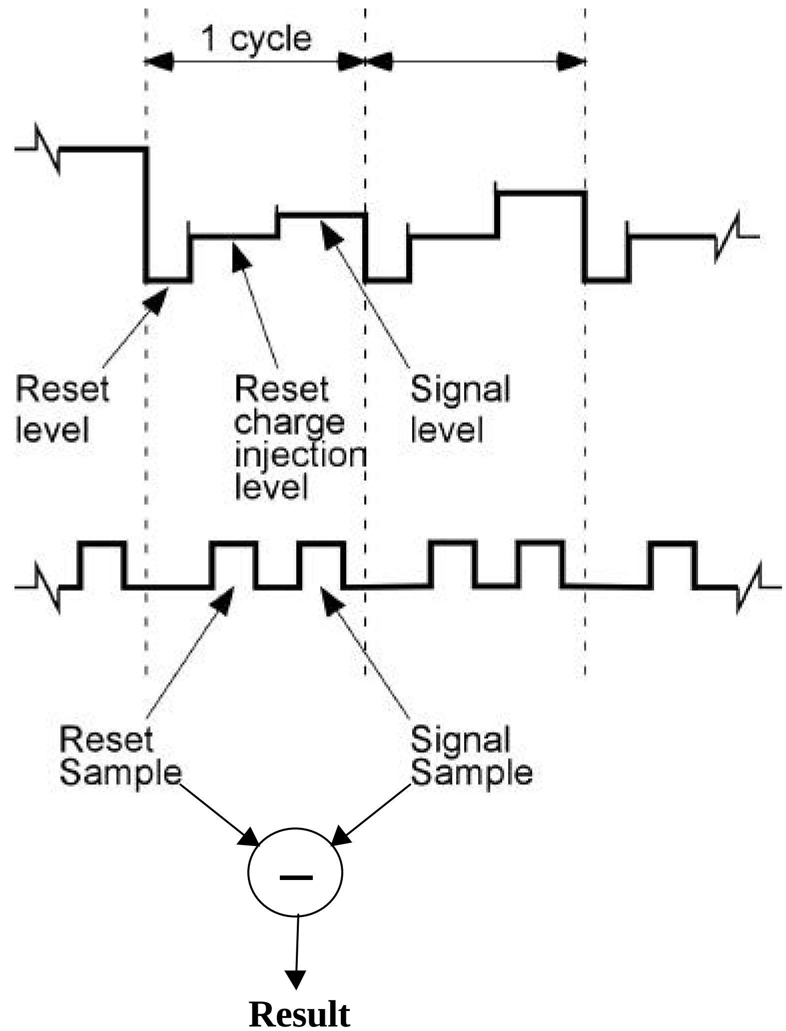
There are many clocks and the voltages are large.

- **Clocks have typical swings of 10V.**
- **FET V_{dd} are 20-25V.**
- **Depletion voltage is up to 80V.**

CCD are anachronisms in the age of deep sub-micron, sub-volt circuitry.

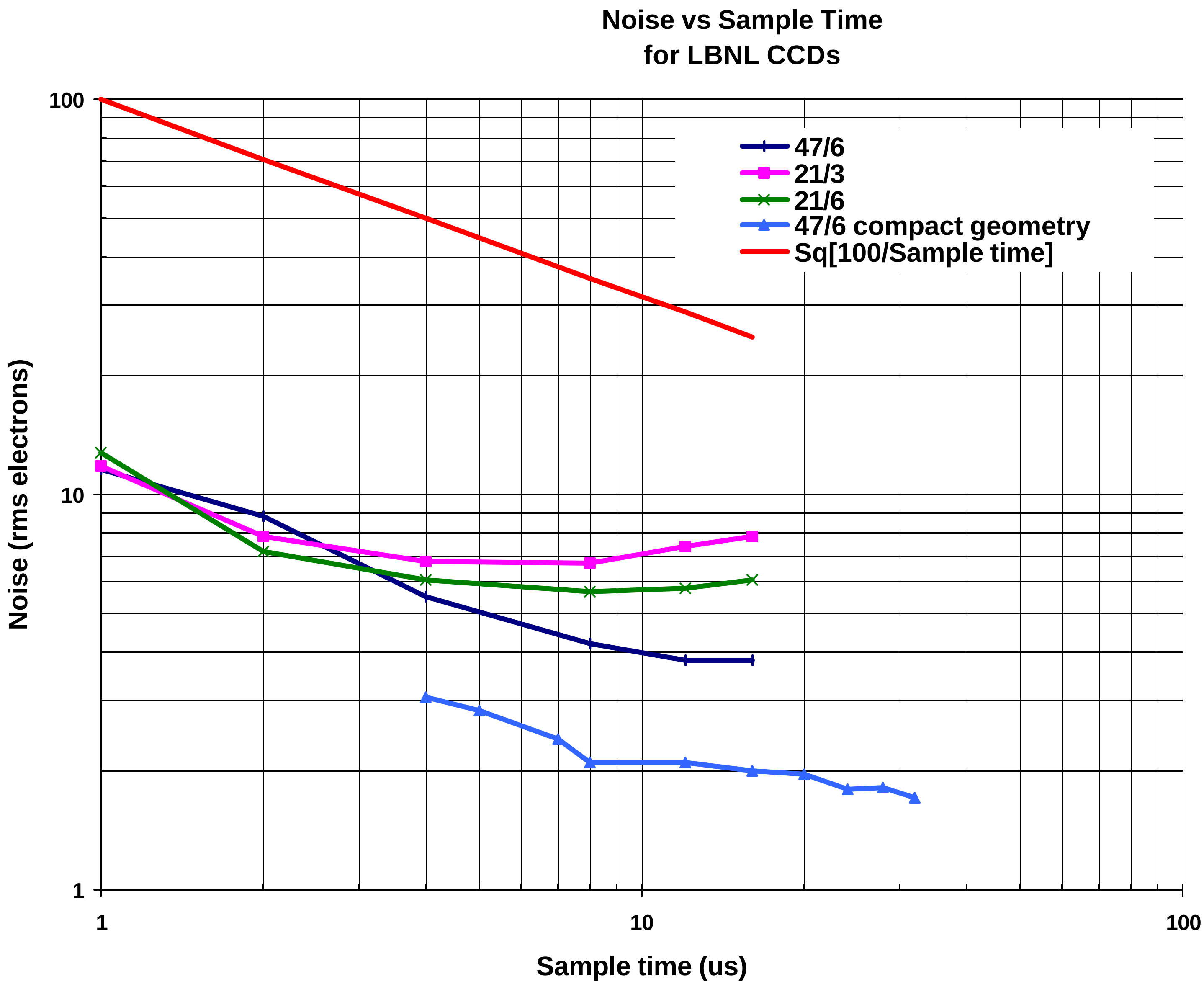
CCD Output Characteristics





Reset kTC noise is ~150e^-.
Read noise is ~2e^- at 50kHz sample rate.
Gain is ~6 μV/e^-.
RL is 5-10kΩ.
Well depth is ~125ke^-.
1/g_m is 3-5kΩ at 1mA and 10V.
16-bit dynamic range is implied.

Read Noise for LBNL CCD



Readout Electronics Concept

•**CDS** – Correlated Double Samples is used for readout of the CCDs to achieve the required readout noise.
– Programmable gain receiver, dual-ramp correlated double sampler, and ADC buffer for each corner of the CCD. HgCdTe compatible.

•**ADC** – 16-bit, 100 kHz equivalent conversion rate per CCD (could be a single muxed 400 kHz unit).

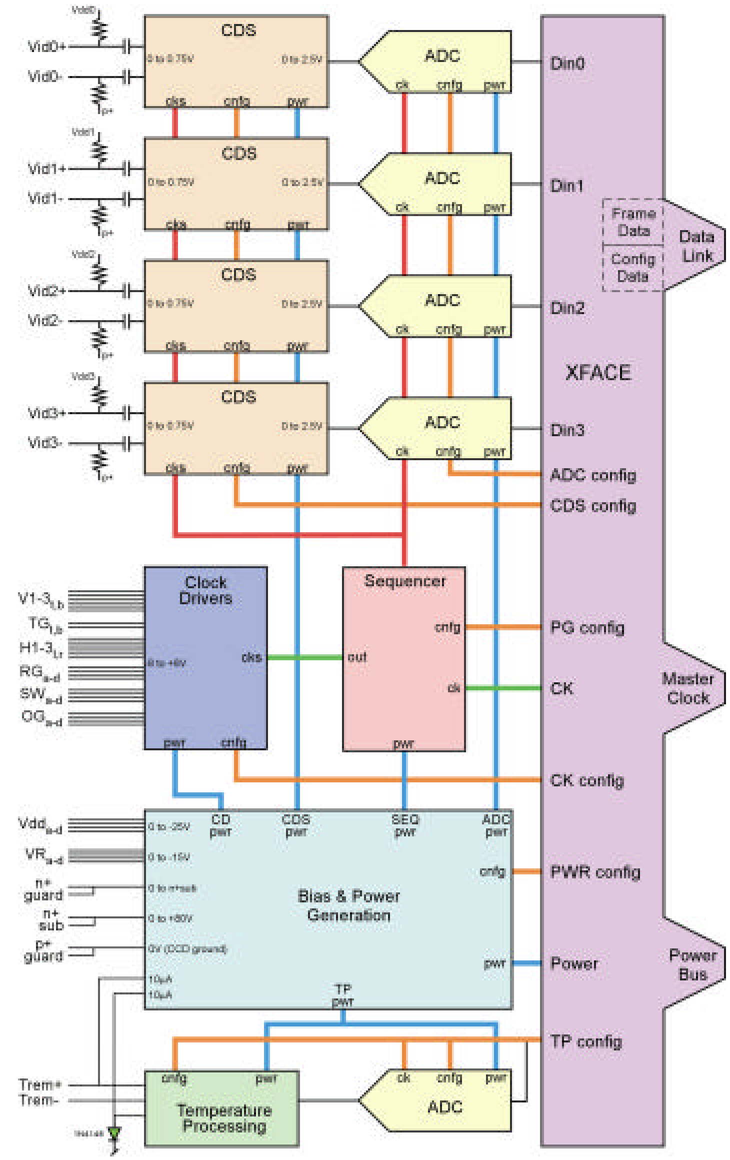
•**Sequencer** – Clock pattern generator supporting modes of operation: erase, expose, readout, idle.

•**Clock drivers** – Programmable amplitude and rise/fall times. Supports 4-corner or 2-corner readout.

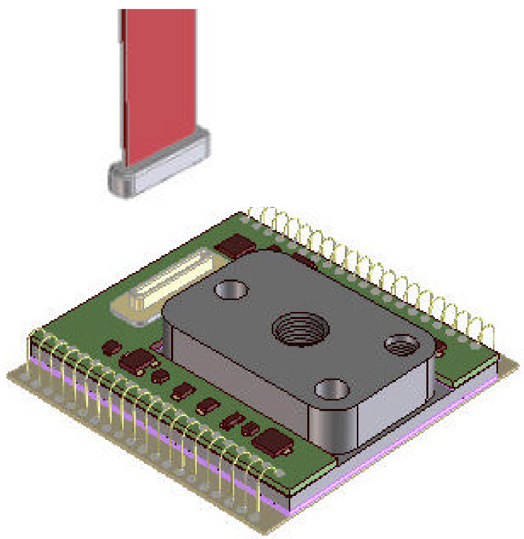
•**Bias and power generation** – Provide switched, programmable large voltages for CCD and local power.

•**Temperature monitoring** – Local and remote.

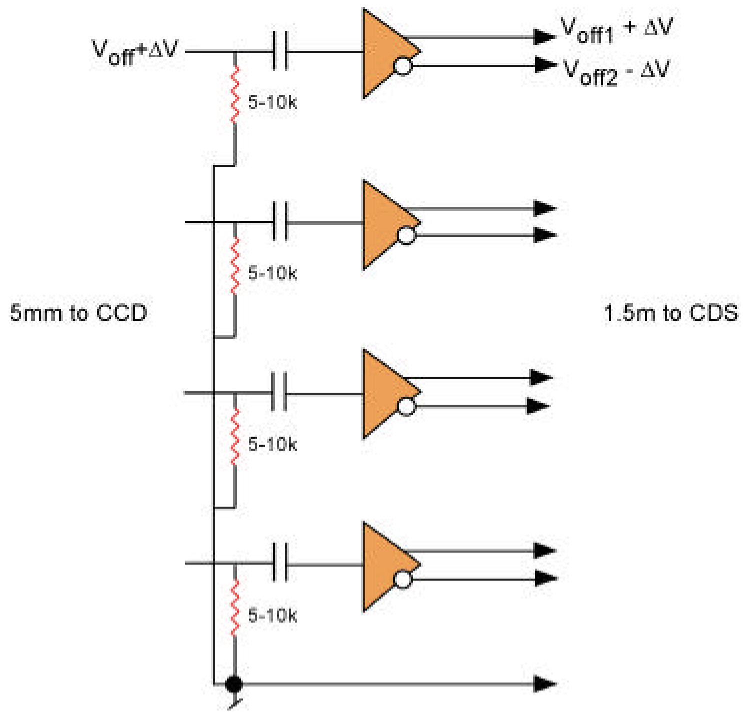
•**DAQ and instrument control interface** – Path to data buffer memory, master timing, and configuration and control.



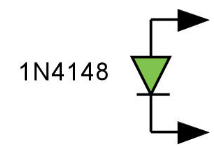
Local CCD Electronics Concept



Cable Driver



Temp. Monitor



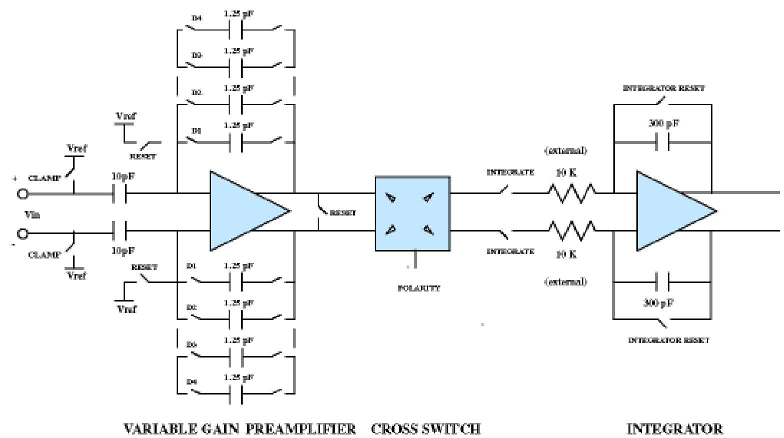
Electronics co-located at the CCD

- **Differential cable driver to help assure noise performance.**
- **Operate first load resistor cold, 150 K.**
- **Provide a temperature monitor.**

ASICs

CDS

Requirements doc done in October 2000 and design submitted in December.



CORRELATED DOUBLE SAMPLER CHIP BLOCK DIAGRAM

First prototype version

Plan for the other parts

- **Before we can proceed, need to complete readout requirements document.**
- **This is supposed to be done in March 2001 and support materials are being gathered, *e.g.*, documenting LBNL CCD clocking needs.**
- **This will be followed by system partitioning, deciding which parts require full custom, FPGA, conventional solutions, *e.g.*, clock shaping. Accessible IC technologies need to considered.**

For details, see Jean-Francois Genat's talk.

LBNL CCD Clock Requirements

(sample requirements documentation)

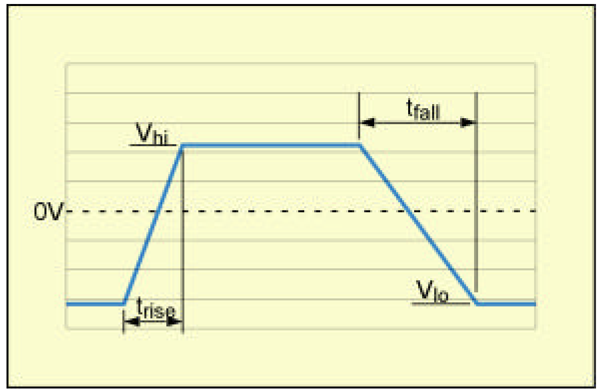
- **Example of material being collected for system requirements document.**
- **The table shows typical and min/max voltages for clocks and bias voltages for modes of operations. Similar tables exist for other devices.**
- **Waveform documentation is also underway.**

LBNL CCD/CDS/ADC voltage ranges

Signal	# of copies	# of wires	Exposure	Readout		Reset		DAC Range		$t_{rise,fall}$ (µsec)	
				Lo	Hi	Lo	Hi	Lo	Hi	min	max
V phi1	2	2	-6.	-6.	+4.	-4.	+6.	-8.	+8.	0	1.00
V phi2	2	2	+4.	-6.	+4.	-4.	+6.	-8.	+8.	0	1.00
V phi3	2	2	+4.	-6.	+4.	-4.	+6.	-8.	+8.	0	1.00
Transfer-gate	2	2	+4.	-6.	+4.	-4.	+6.	-8.	+8.	0	1.00
H phi1	2	2	+6.	-2.	+6.	-2.	+6.	-8.	+8.	0	0.25
H phi2	2	2	-2.	-2.	+6.	-2.	+6.	-8.	+8.	0	0.25
H phi3	2	2	+6.	-2.	+6.	-2.	+6.	-8.	+8.	0	0.25
Output-gate	4	4	+3.5	+3.5	+3.5	+3.5	+3.5	0	+8.	0	0.25
Summing-well	4	4	+5.	-5.	+5.	-5.	+5.	-8.	+8.	0	0.25
Reset gate	4	4	0	-6.	0	-6.	0	-8.	0	0	1.00
Reset drain	4	4	0	-12.5	-12.5	-12.5	-12.5	-15.	0		
Output drain	4	4	0	-21.	-21.	-21.	-21.	-25.	0		
Video out+	4	4	x			x	x				
Video out-	4	4	x			x	x				
n+ substrate	1	2	+60.	+60.	+60.	0	0	0	+80.		
n+ guard	1	2	float	float	float	0	0	0	float		
p+ guard	1	2	0	0	0	0	0	0	0		
Temp mon+	1	1	x	x	x	x	x	-8.	+8.		
Temp mon-	1	1	x	x	x	x	x	x	x		

Clock Shape Generation
(sample partitioning/implementation trade)

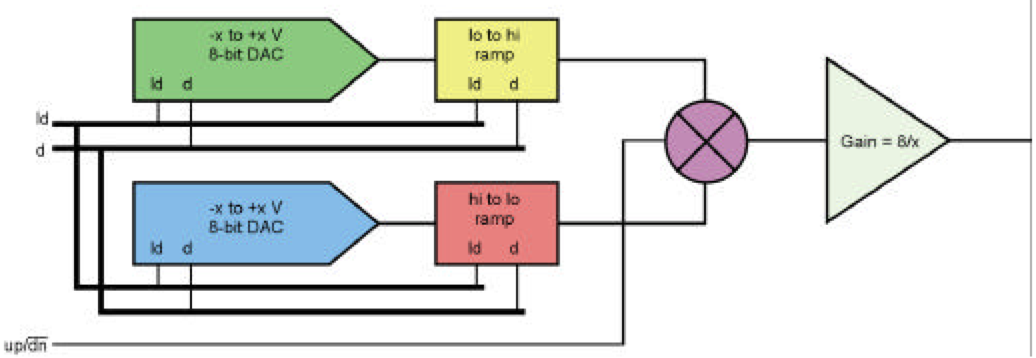
Possible ways to generate clock amplitudes and rise/fall times. To choose a particular approach, tradeoffs between full custom IC, FPGA, and conventional implementations will be made.



High voltage analog IC technology?

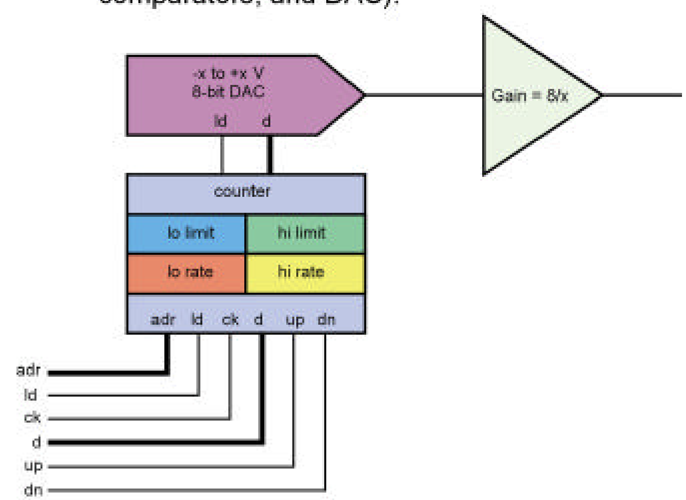
Digital intense IC technology?

DAC toggler



DAC ramper

(counter, rate dividers, comparators, and DAC).

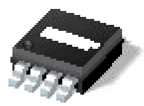


ADC

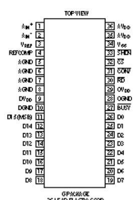
We have a strong preference to purchase this part, not develop a radiation hard custom part.
Why compete with a very active commercial marketplace!

16-bit, ~2.5 V range, 100 kilopixel per second per sensor corner.
Could be a high conversion rate device with input multiplexing.

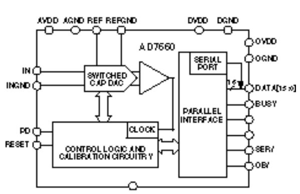
Example devices, by no means exhaustive.



Burr-Brown ADS8320 *et al*.
- 100 kHz, serial output, 8-pin device.
- Very low power 2 mW/10 μW.
- Some BB devices tested at GSFC for GLAST.



Linear Technology LT1604 *et al*.
- 330 kHz requiring input mux, parallel out.
- Modest power 220 mW/10 μW.
- Qualified by SEI for HESSI program.



Analog Devices AD7660 *et al.*
- 100 kHz, parallel/serial out.
- Low power 21 mW/7 μW.
- Some AD devices tested by GSFC for GLAST.

Prototype System

Mid-2003, ASICs and other components will come together for a prototype system test to verify that the requirements are met for the readout electronics.

Components required

- CDS
- Clocking solution
- Bias voltage generation
- Cable technology
- CCD-local electronics
- ADC
- Interface to a computer

Final demonstration is connection to the 4x4 GigaCam demonstration CCD array.

DAQ

Data sources

- **GigaCam** 236 -150 1-MB/s data streams active for 20 s every 120 s.
- **NIR imager** 0.5 MB/s data stream active for 10 s every 100 s.
- **Spectrographs** 0.05 MB/s data stream active for 10 s every 100 s.

On board data buffering

- How do we collect data streams into buffer memory?
- Data will be compressed.

On board data processing

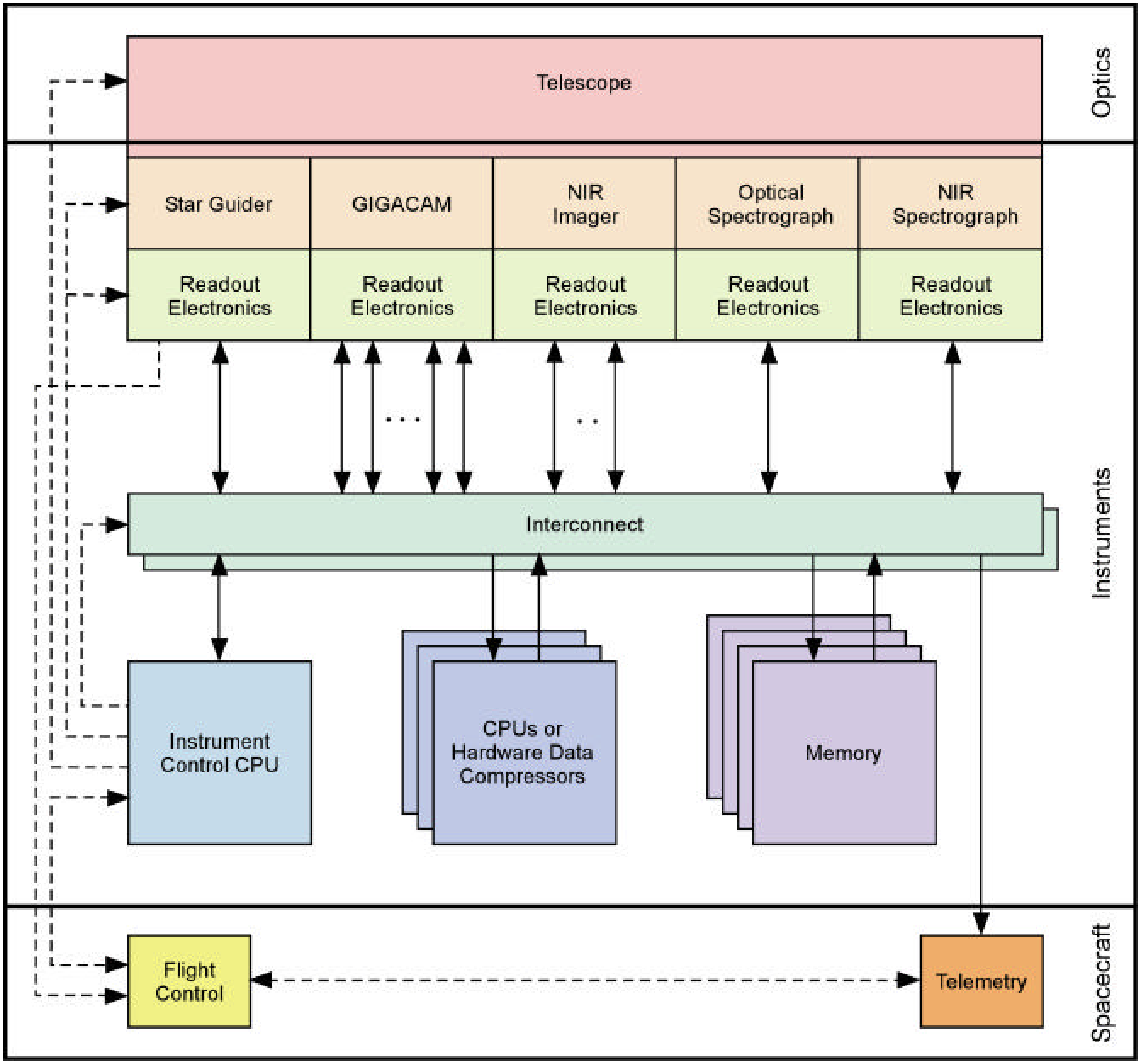
— our preference is to transmit all exposure to ground to allow:

- Different cosmic ray cleanup algorithms,
- Preserve data for continuous calibration using "dark" parts of images,
- Reduce real-time, on-board computing and its software development, especially complex if dithering is used.

Observation program execution

- What will the script directing an observation period look like?
- Where is it executed?
- How are the abstractions turned into instrument control commands.

Instrument Electronics Context

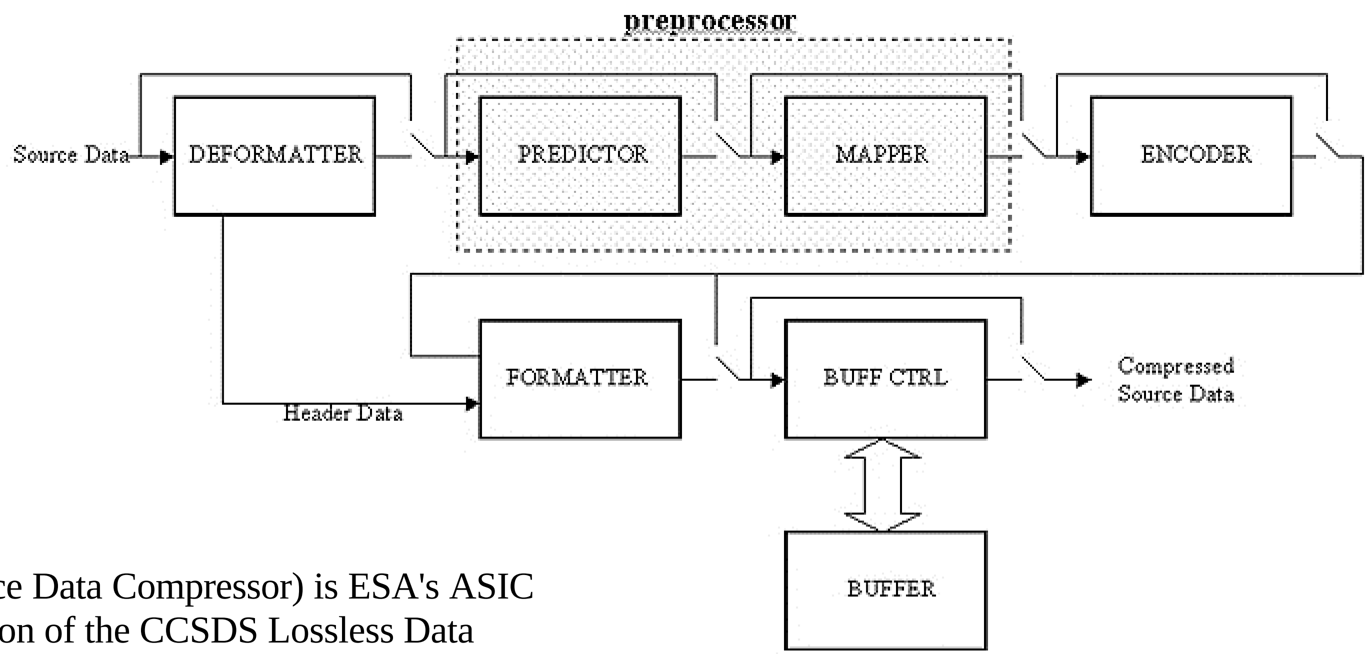


Boundary to be negotiated.

Compression

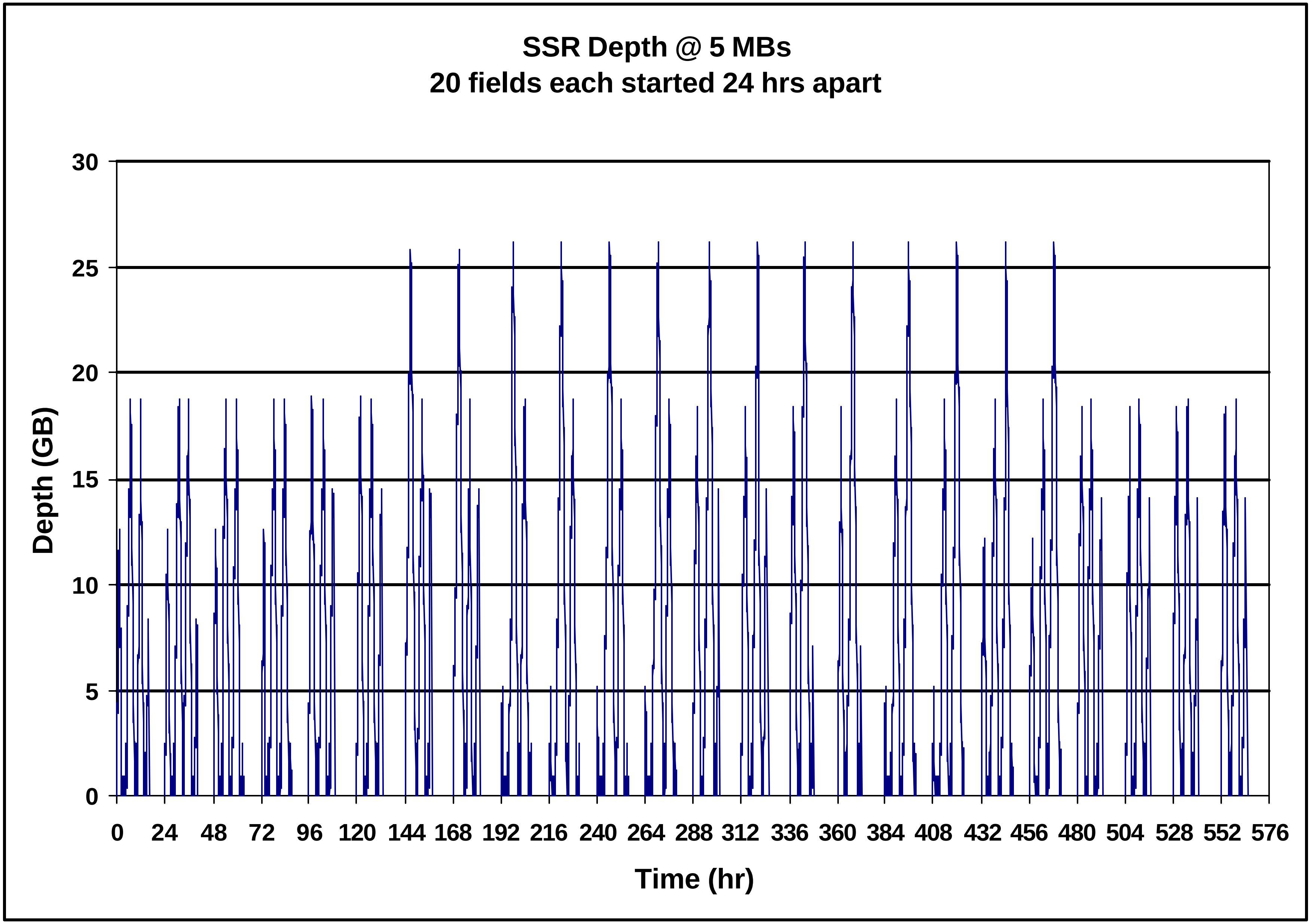
Lossless compression

Rice algorithm much studied for astronomic images.
Factor of 2 gain is conservative – limit is determined by noise.
Available in ASICs, software, and built into memory systems.

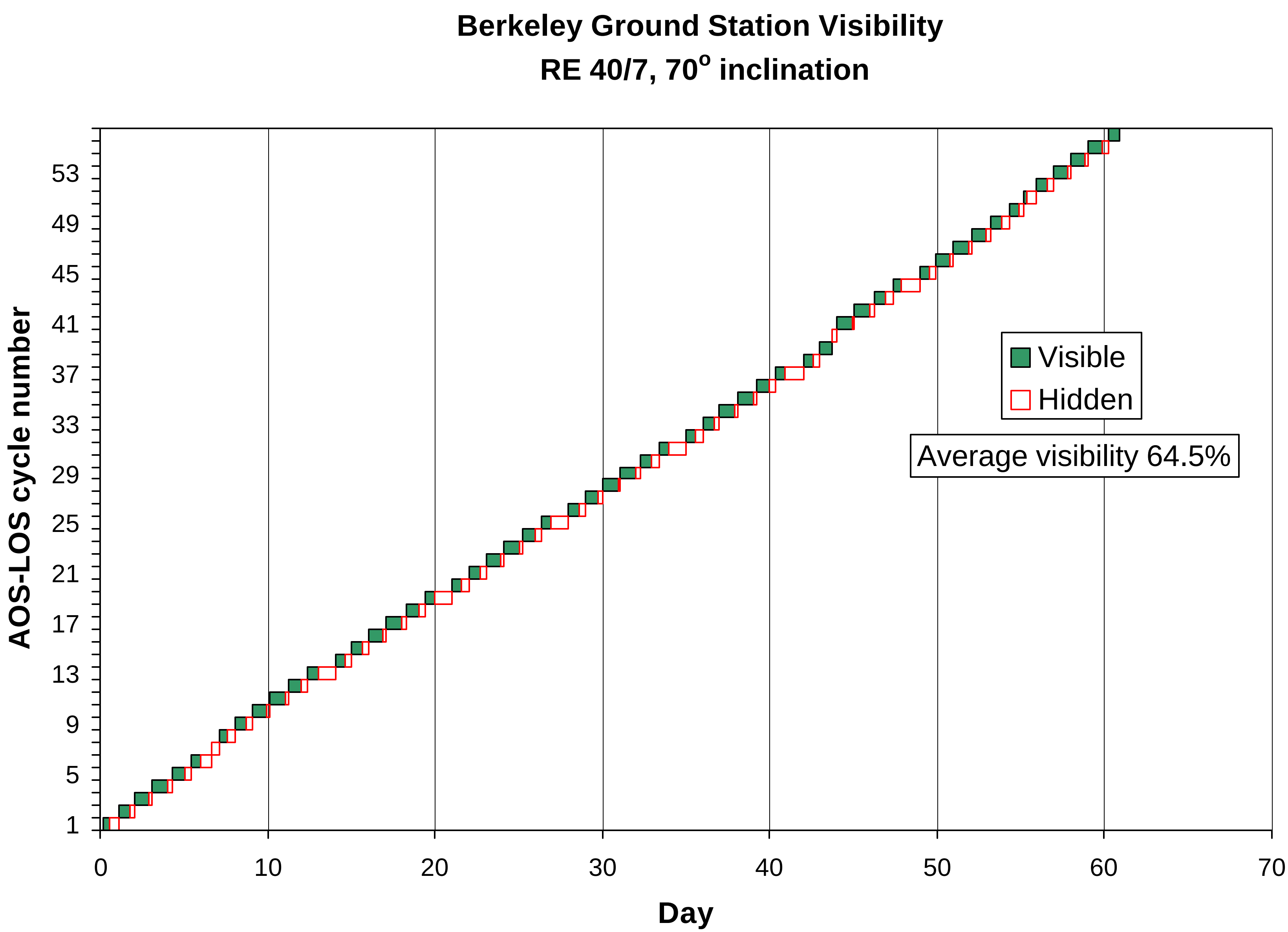


PRDC (Packetizing Rice Data Compressor) is ESA's ASIC hardware implementation of the CCSDS Lossless Data Compression Standard.

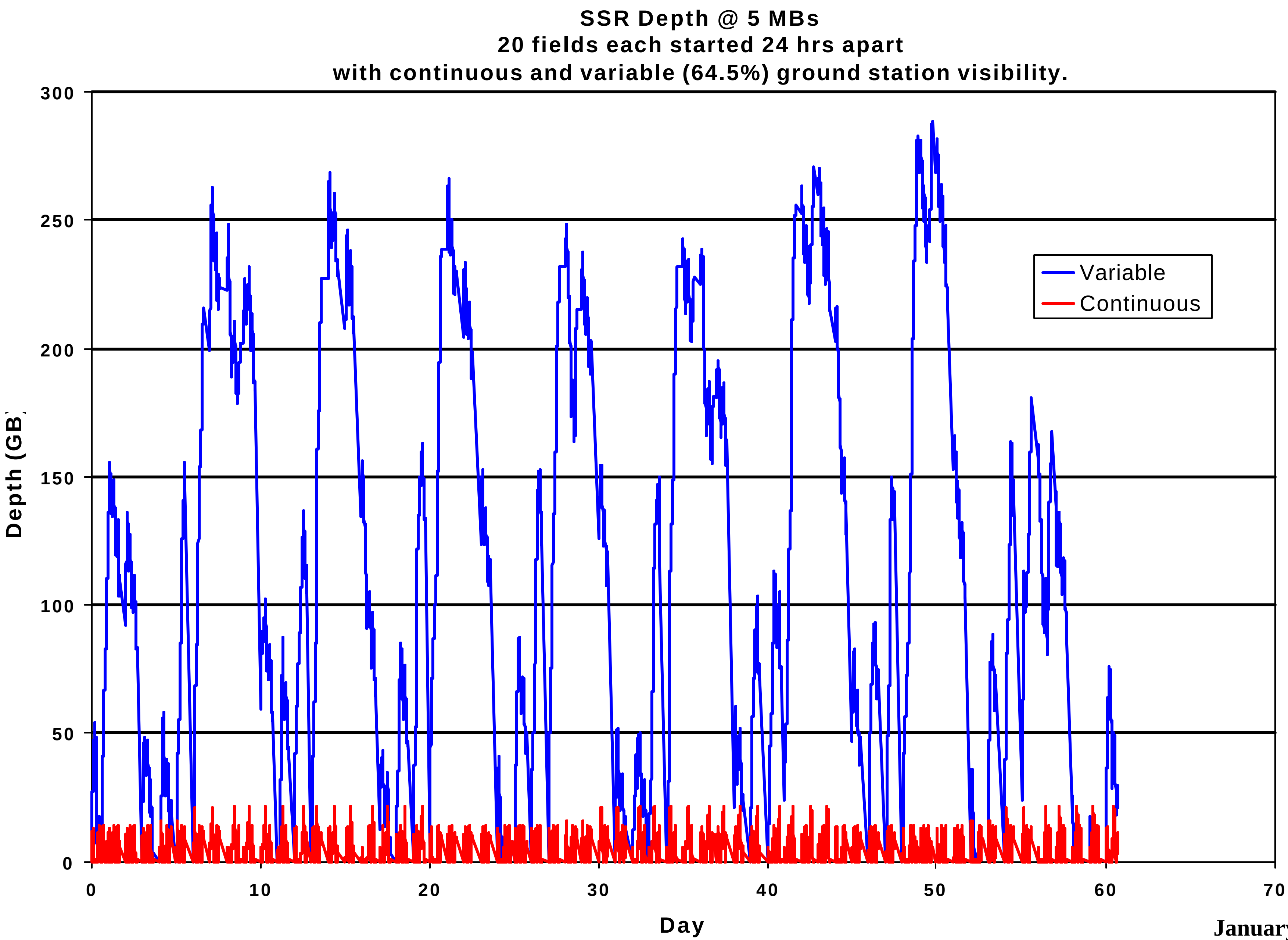
Telemetry vs. Memory Study



Sample Ground Station Visibility



Another Telemetry vs. Memory Study



Instrument Controls

Readout electronics configuration
- DAQ levels
- Clock patterns
- Clock shapes
- FET and depletion voltages
- Mode of operation – idle, expose, erase, readout

Monitoring
- Temperatures
- Local volts and amps

Mechanisms
- Filter wheels
- Shutters
- Lamps
- Rad sources

We note that at this time it is not known that all these items are under the purview of the instruments or the spacecraft.

But the collection of instrument requirements will occur under this activity.

As for readout electronics, we will look for common solutions and implementations.

Management

Requirements driven - generate requirements first.

- Avoid reinvention.
- Guarantee that all issues are identified up front.
- Look for areas where common solutions can be engineered.

Reviews at critical junctures – requirements docs and designs.

- Some reviews are already completed.

Regularly scheduled meetings – this needs to be started.

Summary

We are striving for a coherent solution for readout of all sensors.

- To address space power and space limitations, we have a plan to develop ASICs.
- We are aiming for a mid-2003 system prototype of the readout electronics.

The large volume of data places demands on data buffer size, telemetry rates and ground station availability.

- We are looking for a cost effective solution.

The instruments have control issues.

- We will document these.
- We have an observation program to execute.
- We will work with ground control team to define observation command set.